What is claimed is:

1. A semiconductor device, comprising:

a substrate;

source/drain regions formed in a main surface of said substrate with a channel region interposed therebetween;

a gate insulating film formed on said main surface of said substrate in an area in which said channel region is formed; and

an inversely tapered gate electrode formed on an upper surface of said gate insulating film.

2. A semiconductor device, comprising:

a substrate;

source/drain regions formed in a main surface of said substrate with a channel region interposed therebetween;

a first insulating film formed on said main surface of said substrate in an area in which said source/drain regions are formed;

sidewalls composed of a second insulating film and formed on sides of said first insulating film;

a gate insulating film composed of a third insulating film and formed on said main surface of said substrate in an area in which said channel region is formed; and

a gate electrode formed to fill an inversely tapered recessed portion formed by sides of said sidewalls and an upper surface of said gate insulating film.

3. The semiconductor device according to claim 2, wherein said third

insulating film is composed of a material having a larger dielectric constant than silicon oxide film.

4. The semiconductor device according to claim 3, wherein said third insulating film is one of a tantalum oxide film, a BST film, and a PZT film.

5. The semiconductor device according to claim 3, wherein said third insulating film is formed to extend only onto said sides of said sidewalls.

6. The semiconductor device according to claim 2, further comprising an impurity region locally formed in said substrate only under said gate insulating film and having a conductivity type which is opposite to that of said source/drain regions.

7. The semiconductor device according to claim 2, wherein said source/drain regions are formed in said main surface of said substrate also in areas in which said sidewalls are formed, and

said semiconductor device further comprises an impurity region locally formed in said substrate only under said gate insulating film and said sidewalls and having a conductivity type which is opposite to that of said source/drain regions.

8. The semiconductor device according to claim 2, further comprising a fourth insulating film formed on an upper surface of said gate electrode and surrounding said gate electrode with said sidewalls,

wherein said second and fourth insulating films are composed of a material which is different from that of said first insulating film.

9. The semiconductor device according to claim 2, wherein said gate electrode has its peripheral part formed to extend on an upper surface of said first insulating film.

10. A method for manufacturing a semiconductor device, comprising the steps of:

(a) forming a structure on a main surface of a substrate in an area in which a gate electrode is formed later;

(b) forming source/drain regions in said main surface of said substrate in an area in which said structure is not formed;

(c) forming a first insulating film on said main surface of said substrate in an area in which said structure is not formed;

(d) after said step (c), removing said structure;

(e) forming a second insulating film on the construction obtained by said step (d) and etching said second insulating film by an anisotropic etching whose etching rate is higher in depth direction of said substrate to form sidewalls on sides of said first insulating film;

(f) forming a gate insulating film composed of a third insulating film on said main surface of said substrate in an area in which said first insulting film and said sidewalls are not formed; and

(g) forming said gate electrode to fill an inversely tapered recessed part formed by sides of said sidewalls and an upper surface of said gate insulating film.

11. The semiconductor device manufacturing method according to claim 10,

wherein, in said step (a), said structure is formed by stacking a first film composed of a material which is different from that of said second insulating film and a second film composed of a material which is different from that of said first insulating film in this order, and

said step (d) comprises the steps of;

(d-1) between said step (c) and said step (e), removing said second film with said first film left unremoved, and

(d-2) between said step (e) and said step (f), removing said first film by a wet etching.

12. The semiconductor device manufacturing method according to claim 10, wherein, in said step (a), said structure is formed with a material which is different from that of said first insulating film, and

in said step (d), said structure is removed by a wet etching.

13. The semiconductor device manufacturing method according to claim 10, wherein, in said step (f), said third insulating film is formed with a material having a larger dielectric constant than silicon oxide film.

14. The semiconductor device manufacturing method according to claim 13, wherein said step (f) comprises the steps of;

(x-1) forming said third insulating film on the construction obtained by said step (e), and

(x-2) removing said third insulating film formed on an upper surface of said first insulating film.

15. The semiconductor device manufacturing method according to claim 14, wherein said step (g) comprises the steps of;

(y-1) after said step (x-1), forming a conductor film which is a material of said gate electrode on said third insulating film, and

(y-2) after said step (y-1), thinning said conductor film until said upper surface of said first insulating film is exposed to form said gate electrode,

and wherein said step (x-2) is performed together in the process in which said step (y-2) is performed.

16. The semiconductor device manufacturing method according to claim 14, wherein said step (g) comprises the steps of;

(z-1) after said step (x-1), forming a conductor film which is a material of said gate electrode on said third insulating film, and

(z-2) between said step (z-1) and said step (x-2), thinning said conductor film until said third insulating film formed on said upper surface of said first insulating film is exposed to form said gate electrode,

and wherein, in said step (x-2), said third insulating film is removed by etching said third insulating film exposed in said step (z-2).

17. The semiconductor device manufacturing method according to claim 10, further comprising the step of:

(h) between said step (e) and said step (f), introducing an impurity into said substrate by using said first insulating film and said sidewalls as masks to form an impurity region having a conductivity type which is opposite to that of said source/drain

regions.

18. The semiconductor device manufacturing method according to claim 10, wherein, in said step (b), said source/drain regions are formed to extend also under peripheral part of said structure in said main surface of said substrate, and

said manufacturing method further comprises the step of:

(i) between said step (d) and said step (e), introducing an impurity into said substrate by using said first insulating film as a mask to form an impurity region having a conductivity type which is opposite to that of said source/drain regions.

19. The semiconductor device manufacturing method according to claim 10, wherein said first insulating film is composed of a material which is different from that of said second insulating film, and

said manufacturing method further comprises the steps of;

(j) removing said gate electrode for a given film thickness from its upper surface, and

(k) after said step (j), forming a fourth insulating film composed of a material which is different from that of said first insulating film on said gate electrode.

20. The semiconductor device manufacturing method according to claim 10, wherein said step (g) comprises the steps of;

(g-1) forming a conductor film which is a material of said gate electrode on the construction obtained by said step (f), and

(g-2) patterning said conductor film to form said gate electrode having its peripheral part extending on an upper surface of said first insulating film.